What is claimed is:

1. A correlation detection method capable of creating a delay profile of a reception signal with a delay equivalent to a maximum of X chips (n: natural number), comprising:

a first step of extracting and fixing 1-symbol equivalent data from the data string of said reception signal;

a second step of continuously generating spreading codes with a delay in 1-chip units by changing the amount of phase shift of the spreading codes from 0 chips to X chips, multiplying said fixed data by the spreading codes generated to obtain despreading results, executing integration with respect to said despreading results while changing the integration segments taking into account virtual delimiters of the reception signal symbols which are uniquely determined according to the amount of phase shift of said spreading codes and storing the integration values;

a third step of newly extracting and fixing 1-symbol equivalent data adjacent to said fixed 1-symbol equivalent data and executing the same processing as said processing;

a fourth step of adding up integration values corresponding to the same amount of phase shift of the spreading codes obtained in said second step and said third step, which can be assumed to be the integration

values with respect to the same symbol when virtual delimiters of said reception signal symbols are considered and calculating a correlation value on one symbol; and

a fifth step of comparing among the calculated symbol-unit correlation values and detecting an amount of actual delay of said reception signal by detecting a maximum correlation value.

2. The correlation detection method according to claim 1, wherein a delay profile of a reception signal with a delay longer than a 1-symbol equivalent time by executing said steps using one matched filter.

3. A correlation detection method comprising:

a step of temporarily storing input data and fixing the data and despreading the fixed data while changing the phase of a spreading code;

a step of integrating the despreading result with respect to a first-half symbol segment located before a uniquely determined symbol delimiter according to the amount of phase shift of said spreading code and a last-half symbol segment located after the symbol delimiter; and

a step of adding the integration result of said first-half symbol segment to the integration result corresponding to the same amount of phase shift of said spreading code with respect to the same symbol stored as a result of the same processing as the previous processing, while temporarily storing the integration result of said last-half symbol segment and adding the

stored integration result to the integration result corresponding to the same amount of phase shift of said spreading code with respect to the same symbol obtained as a result of executing the next same processing, and thereby detecting a symbol-unit correlation.

4. The correlation detection method according to claim 3, further comprising a step of comparing among the detected symbol-unit correlation values and detecting the amount of actual delay of said input data by detecting a maximum correlation value.

5. The correlation detection method according to claim 3, wherein serial data with two or more types of signals placed alternately for one chip after another and multiplexed is used as said input data and timings of data processing are controlled according to the level of multiplexing and thereby the processing in said steps is carried out only on the signals subject to correlation detection of said two or more types of signals.

6. A matched filter comprising:

a temporary storage circuit that stores input data;

a spreading code generator that continuously generates spreading codes whose phase is shifted one chip at a time;

a despreading calculation circuit that multiplies said input data stored in said temporary storage circuit by said spreading codes;

an integration circuit that integrates despreading results with respect to a first-half symbol segment

located before a uniquely determined symbol delimiter according to the amount of phase shift of said spreading code and a last-half symbol segment located after the symbol delimiter;

a storage circuit that temporarily stores the integration result of said last-half symbol segment;

a calculation circuit that adds the integration result with respect to said first-half symbol segment to the integration result corresponding to the same amount of phase shift of said spreading code with respect to the same symbol stored in said storing means as a result of the same processing as the previous processing and outputs a correlation value on one symbol.

7. The matched filter according to claim 6, wherein said integration circuit obtains an integration result of said first-half segment by subtracting the integration result of said last-half segment from the integration result obtained by carrying out an integration calculation on all output bits of said despreading calculation circuit.

8. A matched filter comprising:

a temporary storage circuit that stores input data;

a spreading code generator that continuously generates spreading codes whose phase is shifted one chip at a time;

a despreading calculation circuit that multiplies said input data stored in said temporary storage circuit by said spreading codes;

a cumulative addition calculation section that

cumulatively adds up data bits output from said despreading calculation circuit one after another starting from the least significant bit or the most significant bit and outputs a plurality of resulting cumulative addition values in parallel;

a selector that selects said plurality of cumulative addition values output from said cumulative addition calculation section;

a calculation circuit that calculates an integration value of the despreading result with respect to a first-half symbol segment located before a symbol delimiter uniquely determined according to the amount of phase shift of said spreading code by subtracting the cumulative addition value selected by said selector from the integration result obtained by carrying out an integration with respect to all output bits of said despreading calculation circuit; and

a calculation circuit that adds said integration value with respect to said first-half symbol segment to the integration value corresponding to the amount of said phase shift of the spreading code with respect to the same symbol acquired and stored as a result of the same processing as the previous processing and outputs a correlation value on one symbol.

9. A matched filter that extracts and fixes data of a predetermined width from serial data with two or more types of signals placed alternately for one chip after another and multiplexed and despreads this fixed data

by continuously multiplying the fixed data by spreading codes whose amount of shift changes from one chip after another to calculate a correlation value, comprising:

a temporary storage circuit that stores data with said predetermined width;

a spreading code generator that continuously generates spreading codes whose phase is shifted one chip at a time;

a despreading calculation circuit that multiplies said input data stored in said temporary storage circuit by said spreading codes;

an integration circuit that controls data processing timing according to the level of multiplexing of said fixed data and thereby substantially applies signal processing to only signals subject to correlation detection of said two or more types of signals, and obtains integration values by integrating the despreading results with respect to a first-half symbol segment located before a symbol delimiter uniquely determined according to the amount of phase shift of said spreading code on the signals subject to the correlation detection and a last-half symbol segment located after the symbol delimiter;

a storage circuit that temporarily stores the integration result of said last-half symbol segment; and

a calculation segment that adds the integration result of said first-half symbol segment to the integration result corresponding to the amount of the same phase shift of spreading codes on the same symbol

stored in said storing means as a result of the same processing as the previous processing and outputs a correlation value on one symbol.

10. The matched filter according to claim 9, wherein said integration circuit controls the range of integration using a shift register.

11. The matched filter according to claim 10, wherein said integration circuit controls the range of integration using a shift register and an inversion/non-inversion control circuit that controls inversion/non-inversion of the output bits of said shift register.

12. A CDMA reception apparatus comprising the matched filter according to claim 6 that carries out synchronization acquisition processing or synchronization follow-up processing based on the correlation detection result of said matched filter.

13. A mobile communication base station apparatus that acquires synchronization of a spread spectrum modulated signal using the matched filter according to claim 6 and carries out communication control based on the acquired synchronization timing.

14. A mobile communication terminal apparatus that acquires synchronization of a spread spectrum modulated signal using the matched filter according to claim 6 and carries out communication control based on the acquired synchronization timing.